

Day : Thursday
Date: 8/19/2004

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Time: 14:21:39

Inventor Name Search Result

Your Search was:

Last Name = CUMMINGS

First Name = URI

Application#	Patent#	Status	Date Filed	Title	Inventor Name 17
60487536	Not Issued	020	07/14/2003	ASYNCHRONOUS STATIC RANDOM ACCESS MEMORY	CUMMINGS, URI
60352131	Not Issued	159	01/25/2002	ASYNCHRONOUS CROSSBAR CIRCUIT WITH DETERMINISTIC OR ARBITRATED CONTROL	CUMMINGS, URI
60058662	Not Issued	159	09/12/1997	PIPELINED COMPLETION FOR ASYNCHRONOUS COMMUNICATION	CUMMINGS , URI V.
60052714	Not Issued	159	07/16/1997	THE DESIGN OF A ASYNCHRONOUS MIPS R3000 MICROPROCESSOR	CUMMINGS , URI R.
60036243	Not Issued	159	01/24/1997	TRAVELING WAVE REFLECTIVE MODULATORS	CUMMINGS , URI
10667152	Not Issued	030	09/16/2003	ASYNCHRONOUS MULTIPLE-ORDER ISSUE SYSTEM ARCHITECTURE	CUMMINGS, URI
10634597	Not Issued	030	08/04/2003	ASYNCHRONOUS SYSTEM-ON-A-CHIP INTERCONNECT	CUMMINGS, URI
10335343	Not Issued	161	12/31/2002	PIPELINED COMPLETION FOR ASYNCHRONOUS COMMUNICATION	CUMMINGS, URI V.
10294044	Not Issued	020	07/18/2001	RESHUFFLED COMMUNICATIONS PROCESSES IN PIPELINED ASYNCHRONOUS CIRCUITS	CUMMINGS, URI
10237406	Not Issued	020	09/06/2002	ASYNCHRONOUS CROSSBAR WITH DETERMINISTIC OR ARBITRATED CONTROL	CUMMINGS, URI
10237358	Not Issued	020	09/06/2002	ASYNCHRONOUS CROSSBAR WITH DETERMINISTIC OR ARBITRATED CONTROL	CUMMINGS, URI

10137035	6658550	150	04/30/2002	PIPELINED ASYNCHRONOUS PROCESSING	CUMMINGS, URI
10136025	Not Issued	020	04/30/2002	ASYNCHRONOUS CROSSBAR WITH DETERMINISTIC OR ARBITRATED CONTROL	CUMMINGS, URI
09496128	6502180	150	02/01/2000	ASYNCHRONOUS CIRCUITS WITH PIPELINED COMPLETION PROCESS	CUMMINGS, URI V.
09151334	6038656	150	09/11/1998	PIPELINED COMPLETION FOR ASYNCHRONOUS COMMUNICATION	CUMMINGS , URI V.
09118140	6381692	150	07/16/1998	PIPELINED ASYNCHRONOUS PROCESSING	CUMMINGS , URI
08999194	5886807	150	12/19/1997	TRAVELING-WAVE REFLECTIVE ELECTRO OPTIC MODULATOR	CUMMINGS , URI

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Inventor Name Search Result

Your Search was:

Last Name = LINES

First Name = ANDREW

Application#	Patent#	Status	Date Filed	Title	Inventor Name 30
60487536	Not Issued	020	07/14/2003	ASYNCHRONOUS STATIC RANDOM ACCESS MEMORY	LINES, ANDREW
60444820	Not Issued	159	02/03/2003	ASYNCHRONOUS INTERCONNECT SYSTEM	LINES, ANDREW
60429153	Not Issued	159	11/25/2002	MESSAGE UNIT	LINES, ANDREW
60411717	Not Issued	159	09/16/2002	ASYNCHRONOUS MULTIPLE-ORDER ISSUE PROCESSOR ARCHITECTURE	LINES, ANDREW
60408175	Not Issued	159	08/30/2002	PSEUDO-RANDOM DRAM PACKET STORE	LINES, ANDREW
60404359	Not Issued	159	08/15/2002	P2N SIZING TOOL - PATH BASED SIZING	LINES, ANDREW
60403045	Not Issued	159	08/13/2002	IN-LINE ERROR CORRECTION TECHNIQUES IN DATA PROCESSING SYSTEMS	LINES, ANDREW
60357201	Not Issued	159	02/12/2002	ASYNCHRONOUS-SYNCHRONOUS CONVERSION CIRCUITS	LINES, ANDREW
60352131	Not Issued	159	01/25/2002	ASYNCHRONOUS CROSSBAR CIRCUIT WITH DETERMINISTIC OR ARBITRATED CONTROL	LINES, ANDREW
60093840	Not Issued	159	07/22/1998	PIPELINED ASYNCHRONOUS CIRCUITS	LINES , ANDREW M.
60058662	Not Issued	159	09/12/1997	PIPELINED COMPLETION FOR ASYNCHRONOUS COMMUNICATION	LINES , ANDREW M.
60052714	Not Issued	159	07/16/1997	THE DESIGN OF A ASYNCHRONOUS MIPS R3000 MICROPROCESSOR	LINES , ANDREW
10667152	Not	030	09/16/2003	ASYNCHRONOUS MULTIPLE-	LINES, ANDREW

	Issued			ORDER ISSUE SYSTEM ARCHITECTURE	
<u>10634597</u>	Not Issued	030	08/04/2003	ASYNCHRONOUS SYSTEM- ON-A-CHIP INTERCONNECT	LINES, ANDREW
<u>10452782</u>	Not Issued	020	05/30/2003	MESSAGE TRANSFER SYSTEM	LINES, ANDREW
<u>10354272</u>	<u>6785875</u>	150	01/28/2003	METHODS AND APPARATUS FOR FACILITATING PHYSICAL SYNTHESIS OF AN INTEGRATED CIRCUIT DESIGN	LINES, ANDREW
<u>10335343</u>	Not Issued	161	12/31/2002	PIPELINED COMPLETION FOR ASYNCHRONOUS COMMUNICATION	LINES, ANDREW M.
<u>10294044</u>	Not Issued	020	07/18/2001	RESHUFFLED COMMUNICATIONS PROCESSES IN PIPELINED ASYNCHRONOUS CIRCUITS	LINES, ANDREW M.
<u>10281424</u>	Not Issued	030	10/25/2002	TECHNIQUES FOR FACILITATING CONVERSION BETWEEN ASYNCHRONOUS AND SYNCHRONOUS DOMAINS	LINES, ANDREW
<u>10237406</u>	Not Issued	020	09/06/2002	ASYNCHRONOUS CROSSBAR WITH DETERMINISTIC OR ARBITRATED CONTROL	LINES, ANDREW
<u>10237358</u>	Not Issued	020	09/06/2002	ASYNCHRONOUS CROSSBAR WITH DETERMINISTIC OR ARBITRATED CONTROL	LINES, ANDREW
<u>10212574</u>	Not Issued	030	08/01/2002	TECHNIQUES FOR FACILITATING CONVERSION BETWEEN ASYNCHRONOUS AND SYNCHRONOUS DOMAINS	LINES, ANDREW
<u>10137035</u>	<u>6658550</u>	150	04/30/2002	PIPELINED ASYNCHRONOUS PROCESSING	LINES, ANDREW M.
<u>10136025</u>	Not Issued	020	04/30/2002	ASYNCHRONOUS CROSSBAR WITH DETERMINISTIC OR ARBITRATED CONTROL	LINES, ANDREW
<u>09501638</u>	Not Issued	160	02/10/2000	RESHUFFLED COMMUNICATIONS PROCESSES IN PIPELINED ASYNCHRONOUS CIRCUITS	LINES, ANDREW M.
<u>09496128</u>	<u>6502180</u>	150	02/01/2000	ASYNCHRONOUS CIRCUITS WITH PIPELINED COMPLETION PROCESS	LINES, ANDREW M.

09360468	Not Issued	160	07/22/1999	RESHUFFLED COMMUNICATIONS PROCESSES IN PIPELINED ASYNCHRONOUS CIRCUITS	LINES , ANDREW M.
09151334	6038656	150	09/11/1998	PIPELINED COMPLETION FOR ASYNCHRONOUS COMMUNICATION	LINES , ANDREW M.
09118140	6381692	150	07/16/1998	PIPELINED ASYNCHRONOUS PROCESSING	LINES , ANDREW
08010824	5557714	150	01/29/1993	METHOD AND SYSTEM FOR ROTATING A THREE- DIMENSIONAL MODEL ABOUT TWO ORTHOGONAL AXES	LINES , ANDREW

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